REMARKS

Applicants have amended claims 1 through 36 herein and have added claims 37 through 48; thus, claims 1 through 48 are pending in the application. No new subject matter has been introduced by way of the amendments or new claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

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MARKED UP VERSION OF THE AMENDED CLAIMS

1. (Amended) A thermal management system [for an integrated circuit die,] comprising:

a temperature detection element formed directly on [said] an integrated circuit die, [said] the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on [said] the integrated circuit die [and configured], the power modulation element to reduce power consumption of [said] the integrated circuit die in response to [a logical change in state at said] the output of [said] the at least one temperature sensor;

a control element formed directly on [said] the integrated circuit die, [said] the control element including at least one register [providing] to provide an enable/disable bit for [said] the thermal management system; and

a visibility element formed directly on [said] the integrated circuit die [and configured], the visibility element to indicate a status of [said] the output of [said] the at least one temperature sensor.

2. (Amended) The system of claim 1, [said] the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of [said] the integrated circuit die; and

a comparator having one input coupled via a first signal line to [said] the reference voltage source and another input coupled via a second signal line to [said] the programmable voltage source, [said] the comparator [configured] to provide [said logical change in state at said] a signal at the output of [said] the at least one temperature sensor in response to [said] the programmable voltage substantially equaling [said] the reference voltage.

3. (Amended) The system of claim 2, further comprising a pulse dampener coupled to [said] the first signal line [and configured],the pulse dampener to at least partially remove electrical noise from [said] the reference voltage.

4. (Amended) The system of claim 2, further comprising an analog filter coupled to [said] the second signal line and [said] the first signal line, [said] the analog filter [configured] to detect voltage spikes present in [said] the reference voltage and to add substantially identical voltage spikes to [said] the programmable voltage.

5. (Amended) The system of claim 2, further comprising a digital filter coupled to an output of [said] the comparator, [said] the digital filter including an up-down counter [configured] to count clock pulses, [said] the up-down counter [configured] to increment once for each clock pulse detected when [said] the comparator output is at a [logical high] first state and to decrement once for each clock pulse detected when [said] the comparator output is at a [logical low] second state.

6. (Amended) The system of claim 1, [said] the control element further including [another register selected from a group consisting] at least one of a register [configured] to selectively disengage a specified portion of [said] the thermal management system, a register [configured] to enable [said] the thermal management system in response to an occurrence of an external event, a register [configured] to force [said] the thermal management system active while overriding a disable bit provided by [said] the at least one register, and a register [configured] to allow external software and hardware to enable [said] the thermal management system.

7. (Amended) The system of claim 1, [said] the visibility element including at least one [device selected from a group consisting] of a register [configured] to indicate [said] the status of [said] the temperature sensor output, a register [providing] to provide a sticky bit, a counter [configured] to count a number of lost clock cycles resulting from operation of [said] the thermal management system, and circuitry [configured] to generate an interrupt when [said] the output of the at least one temperature sensor [output] transitions to a different [logical] state.

8. (Amended) The system of claim 1, [said] the power modulation element [configured] to reduce the power consumption of the integrated circuit die by performing at least one of [lower] lowering a supply voltage to [said] the integrated circuit die, [lower] lowering a frequency of a clock signal provided by internal clock circuitry on [said] the integrated circuit die, [perform] performing clock gating of [said] the clock signal provided by [said] the internal clock circuitry, [perform] performing clock throttling of [said] the clock signal provided by [said] the internal clock circuitry, selectively [block] blocking clock pulses of [said] the clock signal provided by [said] the internal clock circuitry, [disable] disabling at least one of a plurality of functional units on [said] the integrated circuit die, [limit] limiting instructions sent to at least one of [said] the plurality of functional units on [said] the integrated circuit die, [or change] and changing a behavior of at least one of [said] the plurality of functional units on [said] the integrated circuit die.

9. (Amended) A microprocessor[,] comprising:
a die having a plurality of functional units formed thereon;
internal clock circuitry formed on [said] the die and coupled to at least one of [said] the plurality of functional units; and
a thermal management system formed directly on [said] the die, [comprising:] the thermal management system including
a temperature detection element including at least one temperature sensor having an output;
a power modulation element [configured] to reduce power consumption of at least one of [said] the functional units in response to [a logical change in state at said] the output of [said] the at least one temperature sensor;
a control element including at least one register [providing] to provide an enable/disable bit for [said] the thermal management system; and
a visibility element [configured] to indicate a status of [said] the output of [said] the at least one temperature sensor.

10. (Amended) The microprocessor of claim 9, [said] the at least one temperature sensor comprising:
a reference voltage source providing a reference voltage;
a programmable voltage source providing a programmable voltage proportional to a temperature of [said] the die; and
a comparator having one input coupled via a first signal line to [said] the reference voltage source and another input coupled via a second signal line to [said] the programmable voltage source, [said] the comparator [configured] to provide [said logical change in state at said] a signal at the output of [said] the at least one temperature sensor in response to [said] the programmable voltage substantially equaling [said] the reference voltage.

11. (Amended) The microprocessor of claim 10, further comprising a pulse dampener coupled to [said] the first signal line [and configured], the pulse dampener to at least partially remove electrical noise from [said] the reference voltage.

12. (Amended) The microprocessor of claim 10, further comprising an analog filter coupled to [said] the second signal line and [said] the first signal line, [said] the analog filter [configured] to detect voltage spikes present in [said] the reference voltage and to add substantially identical voltage spikes to [said] the programmable voltage.

13. (Amended) The microprocessor of claim 10, further comprising a digital filter coupled to an output of [said] the comparator, [said] the digital filter including an up-down counter [configured] to count clock pulses, [said] the up-down counter [configured] to increment once for each clock pulse detected when [said] the comparator output is at a [logical high] first state and to decrement once for each clock pulse detected when [said] the comparator output is at a [logical low] second state.

14. (Amended) The microprocessor of claim 9, [said] the control element further including [another register selected from a group consisting] at least one of a register [configured] to selectively disengage a specified portion of [said] the thermal management system, a register [configured] to enable [said] the thermal management system in response to an occurrence of an external event, a register [configured] to force [said] the thermal management system active while overriding a disable bit provided by [said] the at least one register, and a register [configured] to allow external software and hardware to enable [said] the thermal management system.

15. (Amended) The microprocessor of claim 9, [said] the visibility element including at least one [device selected from a group consisting] of a register [configured] to indicate [said] the status of [said] the temperature sensor output, a register [providing] to provide a sticky bit, a counter [configured] to count a number of lost clock cycles resulting from operation of [said] the thermal management system, and circuitry [configured] to generate an interrupt when [said] the output of the at least one temperature sensor [output] transitions to a different [logical] state.

16. (Amended) The microprocessor of claim 9, [said] the power modulation element [configured] to reduce the power consumption of the at least one functional unit by performing at least one of [lower] lowering a supply voltage to [said] the die, [lower] lowering a frequency of a clock signal provided by [said] the internal clock circuitry, [perform] performing clock gating of [said] the clock signal provided by [said] the internal clock circuitry, [perform] performing clock throttling of [said] the clock signal provided by [said] the internal clock circuitry, selectively [block] blocking clock pulses of [said] the clock signal provided by [said] the internal clock circuitry, [disable] disabling at least one of [said] the plurality of functional units on [said] the die, [limit] limiting instructions sent to at least one of [said] the plurality of functional units on [said] the die, [or change] and changing a behavior of at least one of [said] the plurality of functional units on [said] the die.

17. (Amended) A computer system[,] comprising:

at least one memory device coupled to a bus;

at least one microprocessor coupled to [said] the bus and [said] the at least one memory device, [said] the at least one microprocessor [comprising:] including

a die having a plurality of functional units formed thereon;

internal clock circuitry formed on [said] the die and coupled to at least one of [said] the plurality of functional units;

a temperature detection element formed directly on [said] the die, [said] the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on [said] the die [and configured], the power modulation element to reduce power consumption of at least one of [said] the functional units in response to [a logical change in state at said] the output of [said] the at least one temperature sensor;

a control element formed directly on [said] the die, [said] the control element including at least one register [providing] to provide an enable/disable bit [for said thermal management system]; and

a visibility element formed directly on [said] the die [and configured], the visibility element to indicate a status of [said] the output of [said] the at least one temperature sensor, [said] the temperature detection, power modulation, control, and visibility elements comprising a thermal management system for [said] the die.

18. (Amended) The computer system of claim 17, [said] the at least one temperature sensor comprising:

a reference voltage source providing a reference voltage;

a programmable voltage source providing a programmable voltage proportional to a temperature of [said] the die; and

a comparator having one input coupled via a first signal line to [said] the reference voltage source and another input coupled via a second signal line to [said] the programmable voltage source, [said] the comparator [configured] to provide [said logical change in state at said] a signal at the output of [said] the at least one temperature sensor in response to [said] the programmable voltage substantially equaling [said] the reference voltage.

19. (Amended) The computer system of claim 18, further comprising a pulse dampener coupled to [said] the first signal line [and configured], the pulse dampener to at least partially remove electrical noise from [said] the reference voltage.

20. (Amended) The computer system of claim 18, further comprising an analog filter coupled to [said] the second signal line and [said] the first signal line, [said] the analog filter [configured] to detect voltage spikes present in [said] the reference voltage and to add substantially identical voltage spikes to [said] the programmable voltage.

21. (Amended) The computer system of claim 18, further comprising a digital filter coupled to an output of [said] the comparator, [said] the digital filter including an up-down counter [configured] to count clock pulses, [said] the up-down counter [configured] to increment once for each clock pulse detected when [said] the comparator output is at a [logical high] first state and to decrement once for each clock pulse detected when [said] the comparator output is at a [logical low] second state.

22. (Amended) The computer system of claim 17, [said] the control element further including [another register selected from a group consisting] at least one of a register [configured] to selectively disengage a specified portion of [said] the thermal management system, a register [configured] to enable [said] the thermal management system in response to an occurrence of an external event, a register [configured] to force [said] the thermal management system active while overriding a disable bit provided by [said] the at least one register, and a register [configured] to allow external software and hardware to enable [said] the thermal management system.

23. (Amended) The computer system of claim 17, [said] the visibility element including at least one [device selected from a group consisting] of a register [configured] to indicate [said] the status of [said] the temperature sensor output, a register [providing] to provide a sticky bit, a counter [configured] to count a number of lost clock cycles resulting from operation of [said] the thermal management system, and circuitry [configured] to generate an interrupt when [said] the output of the at least one temperature sensor [output] transitions to a different [logical] state.

24. (Amended) The computer system of claim 17, [said] the power modulation element [configured] to reduce the power consumption of the at least one functional unit by performing at least one of [lower] lowering a supply voltage to [said] the die, [lower] lowering a frequency of a clock signal provided by [said] the internal clock circuitry, [perform] performing clock gating of [said] the clock signal provided by [said] the internal clock circuitry, [perform] performing clock throttling of [said] the clock signal provided by [said] the internal clock circuitry, selectively [block] blocking clock pulses of [said] the clock signal provided by [said] the internal clock circuitry, [disable] disabling at least one of [said] the plurality of functional units on [said] the die, [limit] limiting instructions sent to at least one of [said] the plurality of functional units on [said] the die, [or change] and changing a behavior of at least one of [said] the plurality of functional units on [said] the die.

25. (Amended) A method [of performing thermal management on a microprocessor,] comprising:

providing an enable bit to a register [of a thermal management system] to activate [said] a thermal management system of a die;

measuring a temperature on [a] the die [of said microprocessor] with a sensor of [said] the thermal management system;

providing a [logical low] first state at an output of [said] the sensor when [said] the temperature is below a trip point;

providing a [logical high] second state at [said] the sensor output when [said] the temperature equals or exceeds [said] the trip point;

engaging a power reduction mechanism to reduce power consumption of [said] the die in response to [said logical high at said] the sensor output; and

providing an indication of a [logical] status of [said] the sensor output [of said sensor] to an external device.

26. (Amended) The method of claim 25, [said] further comprising engaging [a] the power reduction mechanism [comprising an act selected from a group consisting] to perform at least one of lowering a supply voltage to [said] the die, lowering a frequency of a clock signal provided by internal clock circuitry [of said microprocessor] on the die, performing clock gating of [said] the clock signal provided by [said] the internal clock circuitry, performing clock throttling of [said] the clock signal provided by [said] the internal clock circuitry, selectively blocking clock pulses of [said] the clock signal provided by [said] the internal clock circuitry, disabling at least one of a plurality of functional units on [said microprocessor] the die, limiting instructions sent to at least one of [said] the plurality of functional units on [said microprocessor] the die, and changing a behavior of at least one of [said] the plurality of functional units on [said microprocessor] the die.

27. (Amended) The method of claim 25, [said providing an enable bit to a register of said thermal management system] further comprising providing an enable bit to [said] the register from an external operating system.

28. (Amended) The method of claim 25, further comprising:
engaging [said] the power reduction mechanism for a specified time period;
polling [said] the sensor output after expiration of [said] the specified time period;
engaging [said] the power reduction mechanism for at least another [said] one of the specified time [period] periods when [said] the sensor output exhibits [said logical high] the second state; and
halting [said] the power reduction mechanism when [said] the sensor output exhibits [said logical low;] the first state.

29. (Amended) The method of claim 25, further comprising:
engaging [said] the power reduction mechanism for a specified time period;
continuously polling [said] the sensor output after expiration of [said] the specified time period; and
halting [said] the power reduction mechanism when [said] the sensor output exhibits [said logical low] the first state.

30. (Amended) The method of claim 25, further comprising:
providing [said logical low] the first state at [said] the sensor output when [said] the temperature is below an untrip point, [said] the untrip point less than [said] the trip point; and
halting [said] the power reduction mechanism in response to [said logical low] the first state.

31. (Amended) The method of claim 25, further comprising:
coupling an up-down counter to [said] the sensor output;
incrementing [said] the up-down counter once for every clock pulse of [said] the clock signal provided by [said] the internal clock circuitry when [said] the sensor output exhibits [said logical high] the first state; and
decrementing [said] the up-down counter once for every clock pulse of [said] the clock signal provided by [said] the internal clock circuitry when [said] the sensor output exhibits [said logical low] the second state.

32. (Amended) The method of claim 25, further comprising:
defining a plurality of trip temperatures, a highest of [said] the plurality of trip temperatures corresponding to [said] the trip point;
assigning a plurality of duty cycle values to [said] the plurality of trip temperatures, one duty cycle value of [said] the plurality of duty cycle values corresponding to at least one of [said] the plurality of trip temperatures; and
providing a clock signal from [said] the internal clock circuitry exhibiting [said] the one duty cycle value in response to [said] the temperature substantially equaling [said] that at least one corresponding trip temperature.

33. (Amended) The method of claim 25, further comprising counting a number of clock cycles eliminated from an output of [said] the internal clock circuitry resulting from [said engaging a] engagement of the power reduction mechanism.

34. (Amended) An apparatus[,] comprising:
a temperature detection element, [said] the temperature detection element including at least one temperature sensor having an output;
a power modulation element, [said] the power modulation element to reduce power consumption of an integrated circuit die in response to [a logical change in state at said] the output of [said] the at least one temperature sensor;
a visibility element, [said] the visibility element to indicate a status of [said] the output of [said] the at least one temperature sensor, [said] the visibility element [comprising:] including
a register to indicate [said] the status of [said] the output of the at least one temperature sensor [output];
a register providing a sticky bit;
a counter to count a number of lost clock cycles resulting from operation of [said] the apparatus; and
circuitry to generate an interrupt when [said] the output of the at least one temperature sensor [output] transitions to a different [logical] state.

35. (Amended) The apparatus of claim 34, further including a control element, [said] the control element comprising:
a register [providing] to provide an enable/disable bit for [said] the apparatus;
a register [configured] to selectively disengage a specified portion of [said] the apparatus;
a register [configured] to enable [said] the apparatus in response to an occurrence of an external event;
a register [configured] to force [said] the apparatus active while overriding a disable bit provided at [said] the enable/disable bit; and
a register [configured] to allow external software and hardware to enable [said] the apparatus.

36. (Amended) The system of claim 34, [said] the power modulation element [configured] to reduce the power consumption of the integrated circuit die by performing at least one of [lower] lowering a supply voltage to [said] the integrated circuit die, [lower] lowering a frequency of a clock signal provided by internal clock circuitry on [said] the integrated circuit die, [perform] performing clock gating of [said] the clock signal provided by [said] the internal clock circuitry, [perform] performing clock throttling of [said] the clock signal provided by [said] the internal clock circuitry, selectively [block] blocking clock pulses of [said] the clock signal provided by [said] the internal clock circuitry, [disable] disabling at least one of a plurality of functional units on [said] the integrated circuit die, [limit] limiting instructions sent to at least one of [said] the plurality of functional units on [said] the integrated circuit die, [or change] and changing a behavior of at least one of [said] the plurality of functional units on [said] the integrated circuit die.